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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,537	06/04/2001	Carl J. Radens	FIS920000011US2(13312A)	4948

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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/873,537	Applicant(s) RADENS ET AL.	
	Examiner Monica Lewis	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to the request for reconsideration filed July 25, 2002.

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Priority

3. An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence of the specification or in an application data sheet (37 CFR 1.78(a)(2) and (a)(5)).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 22-24, 26, 27, 29 and 30 are rejected under 35 U.S.C. 103(a) as obvious over Boardman et al. (U.S. Patent No. 5,120,679) in view of Chang (U.S. Patent No. 5,565,703).

In regards to claim 22, Boardman et al. ("Boardman") discloses the following:

a) a substrate having a first level of electrically conductive features (See Column 3 Lines 38-41);

b) a patterned anti-fuse dielectric layer formed on said substrate, wherein said patterned anti-fuse dielectric layer includes an opening to at least one of said first level of electrically conductive features (See Column 2 Lines 20-24);

c) vias, at least one of said vias has a via space formed above said opening (See Figure 3h); and

d) a second level of electrically conductive features (78 and 80) formed in said vias and via spaces (See Figure 3h).

In regards to claim 22, Boardman fails to disclose the following:

a) a patterned interlevel dielectric material formed on said patterned anti-fuse dielectric layer.

However, Chang discloses a dielectric layer disposed over an antifuse layer (See Column 2 Lines 16-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Boardman to include a dielectric layer as disclosed in Chang because it aids in keeping the device from shortening out.

In regards to claim 23, Boardman discloses the following:

a) substrate is composed of an interlevel dielectric material (See Column 2 Lines 54-59).

In regards to claim 23, Boardman fails to disclose the following:

a) a patterned interlevel dielectric material.

However, Chang discloses a dielectric layer disposed over an antifuse layer (See Column 2 Lines 16-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Boardman to include a dielectric layer as disclosed in Chang because it aids in keeping the device from shortening out.

In regards to claim 24, Boardman fails to disclose the following:

a) interlevel dielectric material is composed of an inorganic semiconductor material selected from the group consisting of $Si0_2$, Si_3N_4, diamond, diamond-like carbon and fluorinated doped oxides.

However, Chang discloses a dielectric layer disposed over an antifuse layer (See Column 2 Lines 16-23, Column 3 Lines 59-61 and Column 4 Lines 28 and 29). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify

the semiconductor device of Boardman to include a dielectric layer as disclosed in Chang because it aids in keeping the device from shortening out.

In regards to claim 26, Boardman discloses the following:

a) first and second levels of electrically conductive features are composed of the same or different conductive metal selected from the group consisting of aluminum, tungsten, copper, chromium, gold, platinum, palladium and alloys, mixtures and complexes thereof (See Column 2 Lines 32-36).

In regards to claim 27, Boardman discloses the following:

a) anti-fuse dielectric layer is a dielectric material selected from the group consisting of $Si0_2$, Si_3N_4, Si oxynitrides, amorphous Si, amorphous C, H-containing dielectrics, carbon, germanium, selenium, compound semiconductors, ceramics and anti-reflective coatings (See Column 2 Lines 32-36).

In regards to claim 29, Boardman discloses the following:

a) interconnect level (See Figure 3h).

In regards to claim 29, Boardman fails to disclose the following:

a) a patterned interlevel dielectric material.

However, Chang discloses a dielectric layer disposed over an antifuse layer (See Column 2 Lines 16-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Boardman to include a dielectric layer as disclosed in Chang because it aids in keeping the device from shortening out.

In regards to claim 30, Boardman discloses the following:

a) interconnect level includes a tapered metal contact region (See Figure 3h).

6. Claim 25 is rejected under 35 U.S.C. 103(a) as obvious over Boardman et al. (U.S. Patent No. 5,120,679) in view of Chang (U.S. Patent No. 5,565,703) and Go et al. (U.S. Patent No. 5,592,016).

In regards to claim 25, Boardman fails to disclose the following:

a) interlevel dielectric material is composed of an organic dielectric material selected from the group consisting of polyimides, polyamides, paralyene and polymethylmethacrylate.

However, Go et al. ("Go") discloses a semiconductor device where the dielectric material is composed of polyimides (See Column 4 Lines 39-48). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Boardman to include a dielectric material composed of polyimides as disclosed in Go to resist abrasion.

7. Claim 28 is rejected under 35 U.S.C. 103(a) as obvious over Boardman et al. (U.S. Patent No. 5,120,679) in view of Chang (U.S. Patent No. 5,565,703) and McCollum et al. (U.S. Patent No. 5,770,885).

In regards to claim 28, Boardman fails to disclose the following:

a) anti-reflective coating is silicon oxynitride.

However, McCollum et al. ("McCollum") discloses a semiconductor device where the anti-reflective coating is composed of silicon oxynitride (See Column 6 Lines 39-45). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Boardman to include an anti-reflective coating of silicon oxynitride as disclosed in McCollum because it has a high dielectric constant which ultimately aids in reducing the leakage current while maintaining the same gate capacitance.

Conclusion

8. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Dixit et al. (U.S. Patent No. 5,233,217) discloses a plug contact with antifuse; b) Birkner et al. (U.S. Patent No. 5,293,133) discloses a method of determining an electrical characteristic of an antifuse; c) Lee et al. (U.S. Patent No. 5,447,880) discloses a method for forming an amorphous silicon element; d) Takagi et al. (U.S. Patent No. 5,550,400) discloses a semiconductor device with an antifuse element; e) Iranmanesh (U.S. Patent No. 5,572,062) discloses an antifuse with spacers; f) Zheng et al. (U.S. Patent No. 5,705,849) discloses an antifuse structure; g) Bhattacharyya et al. (U.S. Patent No. 5,811,870) discloses an antifuse structure; h) Yen et al. (U.S. Patent No. 5,825,072) discloses a circuit for esd protection; i) Schuegraf (U.S. Patent No. 5,886,392) discloses a programmable element having controlled resistance; j) Manley (U.S. Patent No. 5,962,911) discloses an amorphous silicon antifuse; k) Lou et al. (U.S. Patent No. 6,110,826) discloses a dual damascene process; l) Shao et al. (U.S. Patent No. 6,124,194) discloses a method of fabricating an antifuse; m) Sanchez et al. (U.S. Patent No. 6,156,588) discloses a method of forming an antifuse; n) Saito (Japan Application No. JP04242871) discloses a fabrication of a semiconductor device; o) Higashimoto (Japan Application No. JP04342938) discloses a fabrication of a semiconductor device; and p) Yuasa et al. (Japan Application No. JP08010213) discloses a semiconductor device and its manufacture.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
August 7, 2002

CARL WHITEHEAD, JR.
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